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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,945	07/31/2001	Yoshitaka Horie	KIX0154-US	1541

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02/07/2003

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EXAMINER

VU, QUANG D

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 02/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/917,945

Applicant(s)

HORIE, YOSHITAKA

Examiner

Quang D Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 11/27/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 17-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-8 and 17 is/are rejected.
- 7) ☒ Claim(s) 3,4,9-11,18 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

Claims 9-10 and 18-19 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 12-14 are directed to a semiconductor device. However, the claimed subject matters in dependent claims 9, 10, 18 and 19 are directed to the method of making a semiconductor device. Therefore, dependent claims 9, 10, 18 and 19 must be amended to place the claims in proper dependent form or the claims must be canceled.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,005,454 to Froloff et al.

Regarding claim 1, Froloff et al. (figure 1) teach a method of making a semiconductor device. The method comprising the steps of: mounting a semiconductor chip (1) on a lower conductor (8), with first solder material (10) applied between the chip (1) and the lower conductor (8); and positioning an upper conductor (7) on the chip (1), with second solder

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material (9) applied between the chip (1) and the upper conductor (7) (column 3, line 22-column 4, line 35).

Since each of the first and second solder materials (10, 9) can be one of the lead (Pb) and tin (Sn) alloy, the second solder material [9] can be tin alloy and the first solder material [10] can be lead. It is inherent to heat up the first and the second solder materials beyond melting points of the respective materials so that the lower and upper conductors can be connected to the chip. It is also inherent to solidify the first and second materials so that the lower and upper conductors can be connected to the chip. It is inherent that the first solder material is caused to solidify earlier than the second solder material in the solidifying step because lead has a higher melting point than tin alloy.

Regarding claim 2, it is inherent that the melting point of the first solder material is higher than the melting point of the second solder material.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,005,454 to Froloff et al. in view of Admitted Prior Art.

Regarding claim 5, Froloff et al. teach a flat lower electrode (6) being connected to the lower conductor (8). Froloff et al. differ from the claimed invention by not showing a

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semiconductor chip includes a protruding upper electrode being connected to the upper conductor. However, Admitted Prior Art (figures 18-19) teaches a semiconductor chip (90) includes a flat lower electrode (90a) and a protruding upper electrode (90b), the lower electrode (90a) being connected to the lower conductor and the upper electrode (90b) being connected to the upper conductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Admitted Prior Art into the method taught by Froloff et al. for better connection between the upper electrode and the chip.

5. Claims 6-8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,005,454 to Froloff et al. in view of US Patent No. 4,994,412 to Kalfus et al.

Regarding claim 6, Froloff et al. differ from the claimed invention by not showing the step of preparing a conductive frame, which includes the lower and the upper conductors. However, Kalfus et al. (figures 5 and 10) teach a conductive frame (120), which includes the lower and the upper conductors (12, 13, 50, 60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a conductive frame, which includes the lower and the upper conductors, of Kalfus et al. into Froloff et al. because the lead frame is a well known structure for supporting the semiconductor device and providing connection between the external device and semiconductor device.

Regarding claim 7, the combined device shows the lower conductor comprises a die pad portion and lower lead portions extending from the die pad portion, the semiconductor chip being mounted on the die pad portion.

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Regarding claim 8, the combined device shows the upper conductor comprises upper lead portions.

Regarding claim 17, Froloff et al. differ from the claimed invention by not showing a step of preparing a conductive frame, which includes a first conductive pattern and a second conductive pattern, the first conductive pattern including the lower conductor, the second conductive pattern including the upper conductor. However, Kalfus et al. (figure 10) teach a step of preparing a conductive frame (120), which includes a first conductive pattern (12, 13) and a second conductive pattern (50, 60), the first conductive pattern (12, 13) including the lower conductor, the second conductive pattern (50, 60) including the upper conductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kalfus et al. into the method taught by Froloff et al. because conductive frame is a well known structure in the art for supporting the semiconductor device and providing connection between the semiconductor device and the external device.

Response to Arguments

Applicant's arguments filed 11/27/02 have been fully considered but they are not persuasive.

It is argued, in page 6 of the remarks, that Froloff et al. do not teach or suggest using a lower melting point solder material for the first solder and a higher melting point solder material for the second solder. The remark of the applicant is not correct because the specification only discloses the first solder (3A) has a higher melting point than that of the second solder (3B). Since each of the first and second solder materials (10, 9) can be one of the lead (Pb) and tin (Sn)

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alloy, the second solder material [9] can be tin alloy and the first solder material [10] can be lead. It is well known in the art that lead has a higher melting point than tin alloy.

It is argued, in page 6 of the remarks, that Froloff et al. do not teach or suggest the first solder material is caused to solidify earlier than the second solder material in the solidifying step. This argument is not convincing because each of the first and second solder materials (10, 9) can be one of the lead (Pb) and tin (Sn) alloy. Therefore, the second solder material [9] can be tin alloy and the first solder material [10] can be lead. Since lead has a higher melting point than tin alloy, lead can solidify earlier than tin alloy in the solidifying step. It is inherent that the first solder material is caused to solidify earlier than the second solder material in the solidifying step.

Allowable Subject Matter

Claims 3-4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the

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organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv

February 5, 2003

Steven Loh